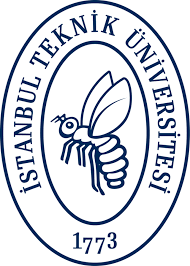
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**DIGITAL SYSTEM DESIGN APPLICATION – EHB 436E**

**Experiment V-Bonus Questions**

**Yiğit Bektaş GÜRSOY**

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1. **SLIDING LEDS**

* Verilog Code

`timescale 1ns **/** 1ps

**module** sliding\_leds**#(**

**parameter** MAX\_CNT\_DEST **=** 500 // 100MHz / 10 = 10M

**)(**

**input** rst**,**clk**,**

**input** **[**1**:**0**]**SW**,**

**output** **reg** **[**15**:**0**]**LED

**);**

**reg** **[**$clog2**(**MAX\_CNT\_DEST**-**1**)-**1**:**0**]** divcounter **=** 0**;**

**reg** divclk**;**

**always** **@(posedge** clk **or** **posedge** rst**)**

**begin**

**if(**rst**)**

LED**<=** 16'h0001**;**

**else**

**begin**

**case(**SW**)**

//stop

2'b00**:**

LED **<=** LED**;**

//10Hz

2'b01**:**

**begin**

**if(**LED **==** 16'h8000**)**

**begin**

**if** **(**divcounter **%** **(**MAX\_CNT\_DEST**-**1**)** **==** 0 **&&** divcounter **!=**0**)**

LED **<=** 16'h0001**;**

**end**

**else**

**begin**

**if** **(**divcounter **%** **(**MAX\_CNT\_DEST**-**1**)** **==** 0 **&&** divcounter **!=**0**)**

LED **<=** LED**<<**1'b1**;**

**end**

**end**

//20Hz

2'b10**:**

**begin**

**if(**LED **==** 16'h8000**)**

**begin**

**if** **(**divcounter **%** **((**MAX\_CNT\_DEST**-**1**)/**2**)** **==** 0 **&&** divcounter **!=**0**)**

LED **<=** 16'h0001**;**

**end**

**else**

**begin**

**if** **(**divcounter **%** **((**MAX\_CNT\_DEST**-**1**)/**2**)** **==** 0 **&&** divcounter **!=**0**)**

LED **<=** LED**<<**1'b1**;**

**end**

**end**

//50Hz

2'b11**:**

**begin**

**if(**LED **==** 16'h8000**)**

**begin**

**if** **(**divcounter **%** **((**MAX\_CNT\_DEST**-**1**)/**5**)** **==** 0 **&&** divcounter **!=**0**)**

LED **<=** 16'h0001**;**

**end**

**else**

**begin**

**if** **(**divcounter **%** **((**MAX\_CNT\_DEST**-**1**)/**5**)** **==** 0 **&&** divcounter **!=**0**)**

LED **<=** LED**<<**1'b1**;**

**end**

**end**

**default** **:** LED **<=** LED**;**

**endcase**

**end**

**end**

**always** **@(posedge** clk **or** **posedge** rst**)**

**begin**

**if(**rst**)**

divcounter **<=**0**;**

**else**

**begin**

**if** **(**divcounter **==** MAX\_CNT\_DEST**)**

divcounter **<=** 0**;**

**else**

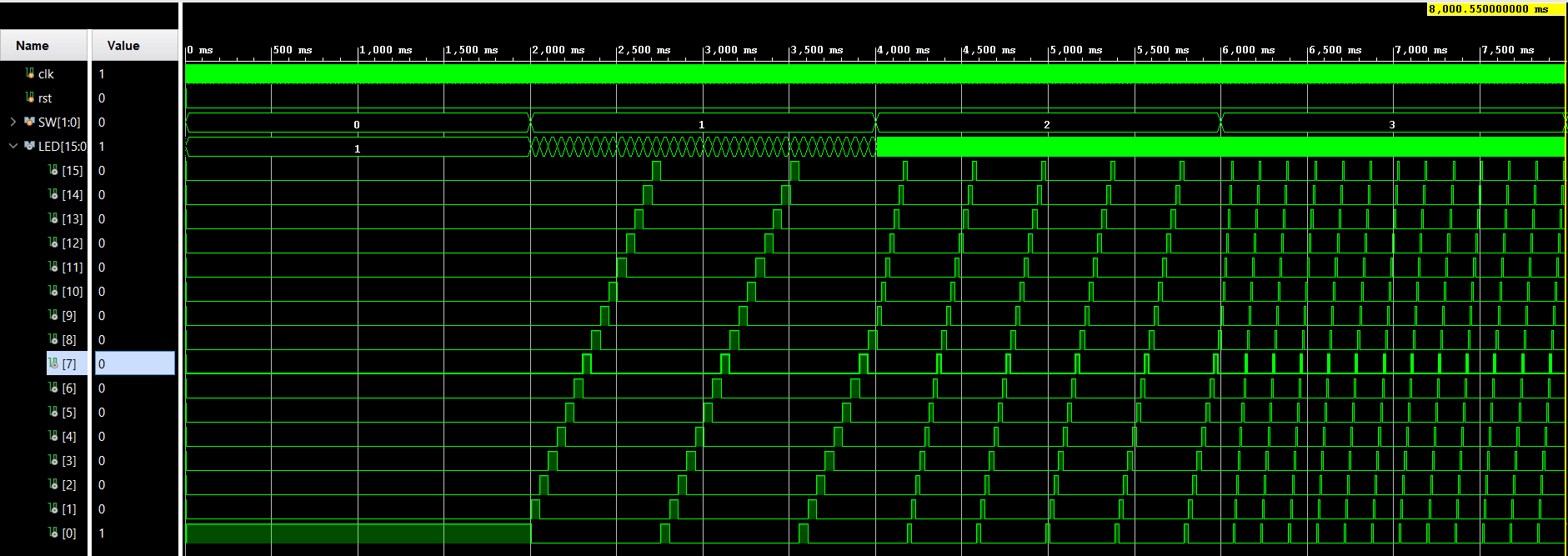
divcounter **<=** divcounter**+**1**;**

**end**

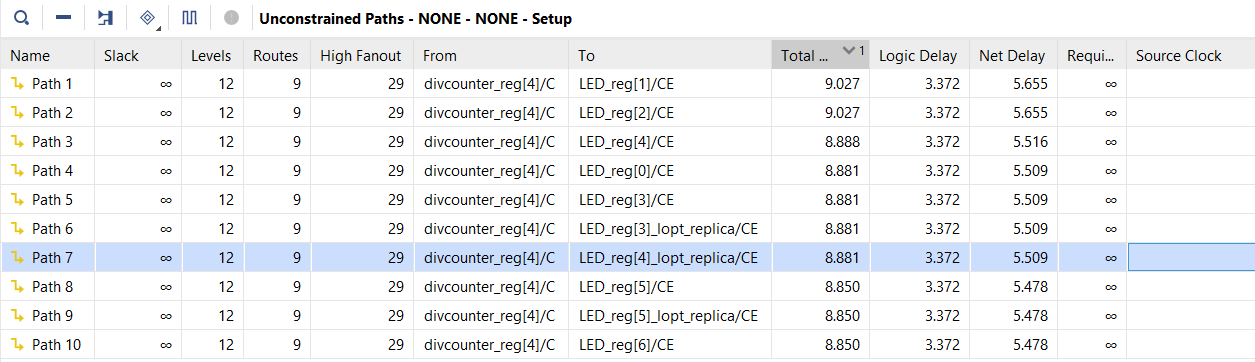
**end**

**endmodule**

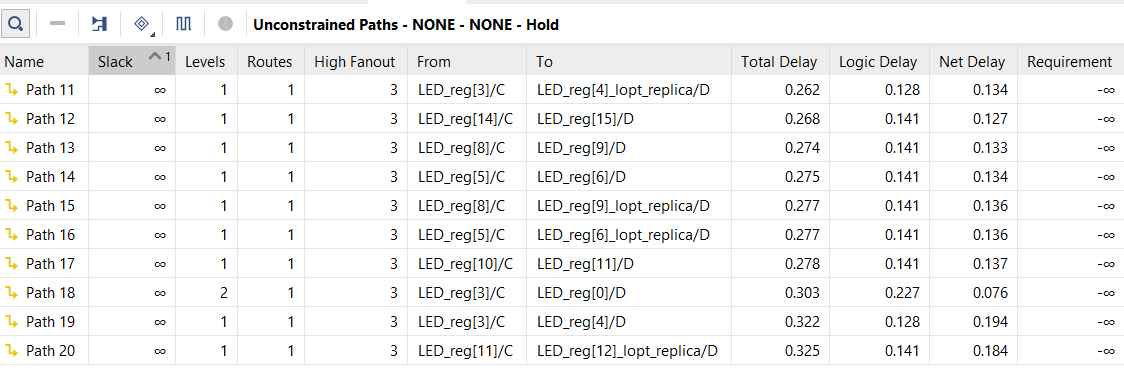
* Behavioral Simulation
* Our input named clk specifies the fpga clk. Our rst input initializes the system and lights the first led. Our SW inputs change the flashing speed of the leds (50Mhz, 20Mhz, 10Mhz), and in the 00 state, the leds keep their last state. As seen in the simulation, the frequencies of the LEDs increased and took up less space in the simulation. Frequency speeds can be controlled with switches.

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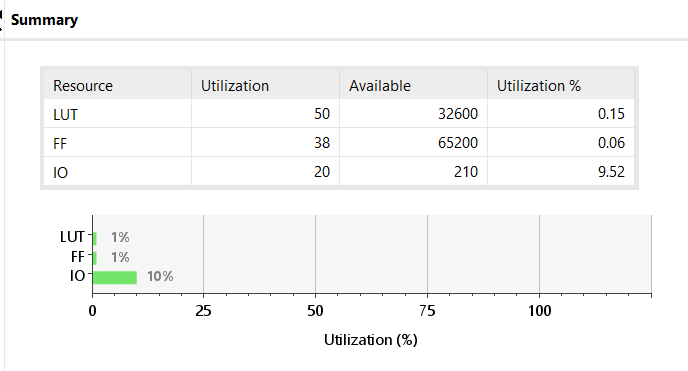
* Realization
* Frequency adjustment was made with the switch case structure. An rst definition was made before these cases started, the rst state is set to 1 before the program starts. In addition to this structure, there is always block where the frequency rate is set.
* Utilization report and critical path slack
* Setup Time

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* Hold Time

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* Utilization Summary



* There are 50LUT , 38FF(flip-flop) and 20IO (input-out) in usage in our device.